

Distinguished Lectures HG01 – HG03

Prof. Ian A. Galton, Full Professor, IEEE Fellow,
Head of Integrated Signal Processing Group,
University of California, San Diego, USA

- **Mismatch-Shaping Techniques for Delta-Sigma Data Converters** 23/7 09:30
- **Digital Background Calibration in Pipelined ADCs** 23/7 15:15



Prof. Bram Nauta, Full Professor, IEEE Fellow,
Head of IC Design Group,
University of Twente, The Netherlands

- **Ultra low-power & Wideband High-speed Nyquist AD Converter** 22/7 18:30
- **RF Circuit Techniques in Nanometer CMOS** 23/7 11:15



Prof. Akira Matsuzawa, Full Professor, IEEE Fellow,
Head of Matsuzawa and Okada Laboratories,
Tokyo Institute of Technology, Japan

- **Low Voltage and Low Power ADC Design** 22/7 16:30
- **The Interpolated Pipeline Method; a New AD Conversion Architecture** 17:30
- **CMOS mm-wave Transceiver Design** 23/7 09:30



Prof. Boris Murmann, Associate Professor,
Head of Mixed Signal Integrated Circuit Design Group,
Stanford University, USA

- **Analysis and Design of Switched-Capacitor Circuits** 23/7 09:30
- **Design of Pipelined A/D Converters** 23/7 11:15
- **Digitally Assisted Data Converter Design** 23/7 17:15



PhD Oral Defenses

IMPORTANT EVENT - PhD Oral Defenses on Microelectronics 22-July 2011

Opening and Live Demo – Location: State Key Lab. of Analog and Mixed-Signal VLSI, JLG212
10:15 Live Demo & Evaluation of Data Converter Measurements by PhD Candidates

PhD Oral Defense Venue: Senate Room, T303, 3/F, Tai Fung Building

Committee Chair: Prof. Simon Ho, Vice Rector (Academic Affairs), UM

External Examiners: Prof. Ian Galton, Prof. Bram Nauta, Prof. Akira Matsuzawa and Prof. Boris Murmann

Internal Examiner: Prof. Mang-I Vai

Supervisor: Prof. Seng-Pan U

Co-Supervisor: Prof. Rui Paulo Martins

Title: High Speed Power / Area Optimized Multi-Bit / Cycle SAR ADCs

Candidate: He-Gong Wei 22/7 11:30, T303

Title: Circuit Techniques for High-Performance SAR Type ADCs

Candidate: Yan Zhu 22/7 14:00, T303



State Key Lab of Analog and Mixed-Signal VLSI - Science Series
First Distinguished Lectures, PhD Oral Defenses & Lab Workshop
22-23 July 2011, University of Macau, Macao, China

Distinguished Lectures & Lab Workshop

Time and Location	Event	Presented by
22-July		
Opening – Location: State Key Lab. of Analog and Mixed-Signal VLSI, JLG212		
22-July 09:30 JLG213	Opening Address - State-Key Lab Establishment & Future Perspective	Prof. Rui Martins
22-July 09:45 JLG213	UM Analog Integrated Circuit Research - Evolution and Results	Prof. Seng-Pan U
22-July High Efficiency Low Power Data Converters (16:00 – 19:30, 16:00 – 16:30 Coffee break)		
22-July 16:30 HG02	Low Voltage and Low Power ADC Design	Prof. Akira Matsuzawa
	The Interpolated Pipeline Method; a New AD Conversion Architecture	Prof. Akira Matsuzawa
	Ultra Low-power & Wideband High-speed Nyquist AD Converter	Prof. Bram Nauta
23-July		
23-July 08:45 HG02	Briefing of Research Activities of Wireless Research Line	Dr. Pui-In Mak
23-July 09:05 HG02	Briefing of Research Activities of Data Conversion and Signal Processing Research Line	Dr. Sai-Weng Sin
23-July Morning Parallel Sessions (09:30-12:45, 11:00-11:15 Coffee break)		
Session 1: Oversampling Data Converters		
23-July 09:30 HG01	Mismatch-Shaping Techniques for Delta-Sigma Data Converters	Prof. Ian Galton
Session 2: SC Circuits & Nyquist Rate Data Converters		
23-July 09:30 HG02	Analysis and Design of Switched-Capacitor Circuits	Prof. Boris Murmann
23-July 11:15 HG02	Design of Pipelined A/D Converters	Prof. Boris Murmann
Session 3: RF and mm-wave Circuits		
23-July 09:30 HG03	CMOS mm-wave Transceiver Design	Prof. Akira Matsuzawa
23-July 11:15 HG03	RF Circuit Techniques in Nanometer CMOS	Prof. Bram Nauta
Afternoon Sessions (15:15 - 18:30, 17:00-17:15 Coffee break)		
23-July 15:15 HG02	Digital Background Calibration in Pipelined ADCs	Prof. Ian Galton
23-July 17:15 HG02	Digitally Assisted Data Converter Design	Prof. Boris Murmann



Open to public. For Enquiry: State Key Laboratory of Analog and Mixed-Signal VLSI, JLG212
Tel.: (853) 8397-8796
http://www.fst.umac.mo/en/lab/ans_vlsi/