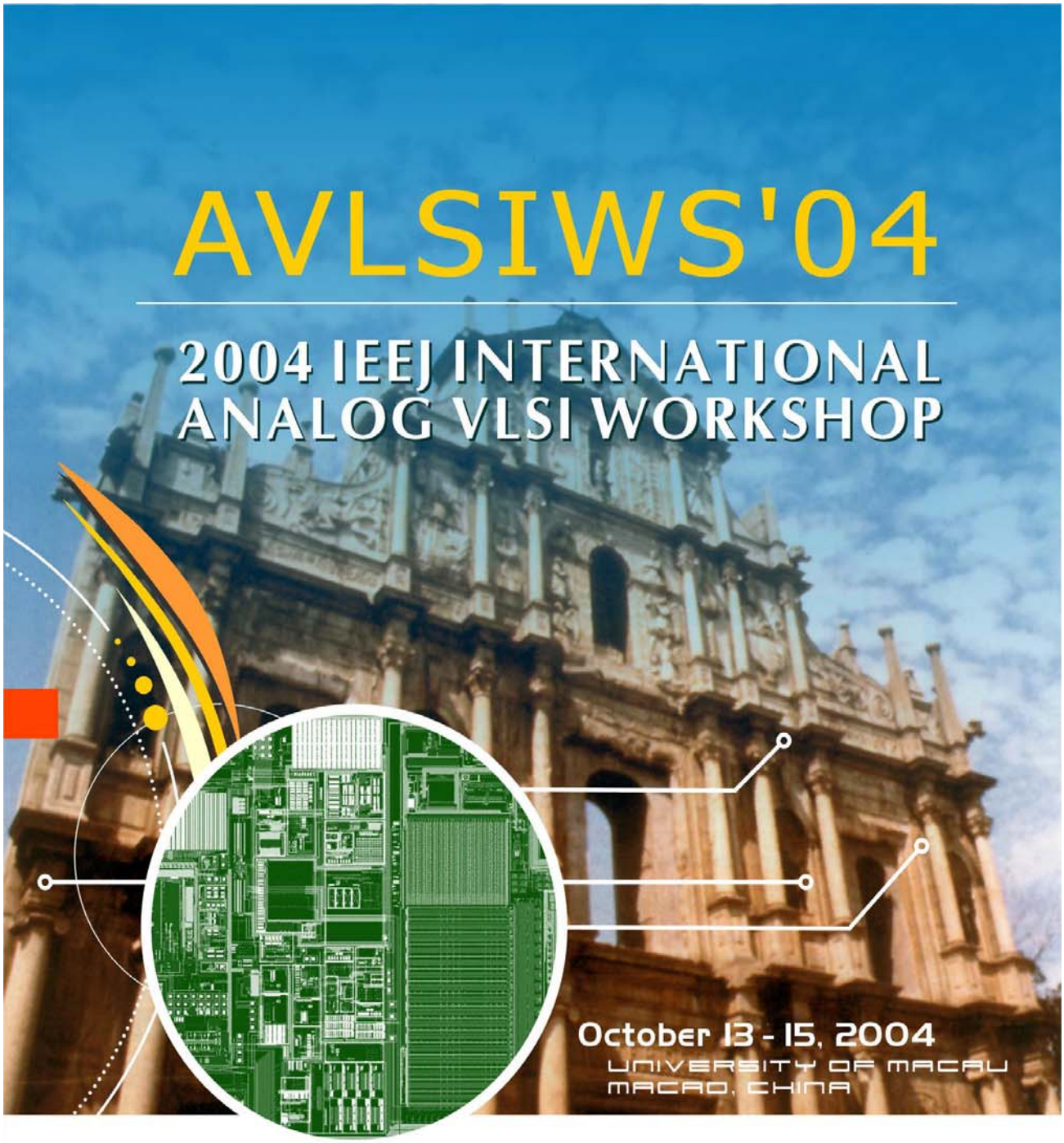

Final Program

Organized by:

Institute of Electrical Engineers of Japan

澳門大學
UNIVERSIDADE DE MACAU

In Collaboration with:

Chipidea Microelectronics (Macau) Limited

IEEE Macau Section

Session Chairman	Day	Time	Title	Author
Special Session 1 Chair: Local Official	13	9:00	Opening Ceremony	
Special Session 2 Chair: Keitaro Sekine	13	9:40	Analog Technologies for the Ubiquitous Society of the Future	Dr. Masao Hotta (General Manager, Renesas Technology Corp, Japan)
Coffee Break		10:30		
Special Session 2 Chair: Rui Martins	13	10:50	Vision about the Role of Analog and Mixed-Signal Design in the Future IC Industry	Prof. José Franca (President & CEO, Chipidea Microelectronica, SA., Portugal)
		11:40	Data Converters for Communications: Opportunities and Challenges for Architectures and Analog Design	Prof. Franco Maloberti (Chair Professor, University of Texas at Dallas, USA)
Lunch		12:30		
Analog Building Blocks 1 Chairs: Cosy Muto & Mang-I Vai	13	14:00	Four-quadrant Multiplying Approach with Low Distortion Voltage-to-Current Convertor in Saturation	Masakazu Mizokami, Kawori Takakubo, and Hajime Takakubo (Chuo University)
		14:20	Low Distortion OTA with MOSFETs Operating in Deep Triode Region	Kawori Takakubo, Shunsuke Ikeda, and Hajime Takakubo (Meiji University)
		14:40	The Design of a High-speed Low-power CMOS Current Comparator	X.M. Wang, and H.L. Kwok (University of Victoria)
		15:00	A Novel Clock Booster Circuit with a Variable Boosting Ratio	Hirokazu Shimizu, Akira Hyogo, and Keitaro Sekine (Tokyo University of Science)
		15:20	Low-Voltage Single-Ended Biquad Low-Pass Filter Using Switched-Opamp and The Simulation Method by This Macro Model	Takahiro Ishii, Hirokazu Shimizu, Akira Hyogo, Koji Tomioka, Tsuyoshi Kaneko and Keitaro Sekine (Tokyo University of Science)
Coffee Break		15:40		
Oscillator Chairs: Masayuki Katakura & Kam-Weng Tam	13	16:00	Phase Noise Characteristics in Extremely Low Phase Noise Oscillator	Yukinori Sakuta, and Yoshihumi Sekine (Nihon University)
		16:20	MOS Transistor Oscillator with Linear Current-Frequency Characteristic	Kazuya Yoshizaki, Shigetaka Takagi, and Nobuo Fujii (Tokyo Institute of Technology)
		16:40	Analysis and Measurement of Injection-Lockable Oscillators for High Gain, High Q Applications	Peter Popplewell, Rony E. Amaya, Mark Cloutier, and Calvin Plett (Carleton University)
		17:00	A 2-GHz CMOS Complimentary LC Voltage Controlled Oscillator with Quadrature Outputs	Ryutaro Saito, Akira Hyogo, and Keirato Sekine (Tokyo University of Science)
		17:20	A Performance Prediction of Clock Generation PLLs: A Ring Oscillator Based PLL and An LC Oscillator Based PLL	Takahito Miyazaki, Masanori Hashimoto, and Hidetoshi Onodera (Kyoto University)
		17:40	Novel Architecture for Ultra Low Complexity Mixed-Signal DLL	Gordon Allan, and John Knight (Carleton University)
Welcome Dinner	13	18:30		

Analog Building Blocks 2 Chair: Akira Hyogo	14	9:00	Low Voltage Compressing Circuit for Voltage Feedback Type Companding Integrator	Makoto Yamagata, and Nobukazu Takai (Tokyo Polytechnic University)
		9:20	CMOS Log-Domain Integrator with DC Gain Improved	Ippei Akita, Kazuyuki Wada, and Yoshiaki Tadokoro (Toyohashi University of Technology)
		9:40	CMOS Linear-Voltage-Output Temperature Sensor based on Characteristic of Zero-Temperature-Coefficient Point	Hidetoshi Ikeda, Kawori Takakubo, and Hajime Takakubo (Chuo University)
		10:00	On the Performance and Use of the Improved Source Follower Buffer	Harri Rapakko, and Juha Kostamovaara (University of Oulu)
Coffee Break		10:20		
Poster Session Chair: Shigetaka Takagi	14	10:40	A Charge Control Model of Power BJTs	Dzhekov A. Tomislav, and Raleva J. Katerina (Cyril and Methodius University)
			Low-Voltage Current Feed-back Amplifier	Kobchai Dejhan, and Sompong Wisetphanichkij (King Mongkuit's Institue of Technolygy, Ladkrabang (KMITL))
			A Low Voltage MOS Translinear Loop Using Current-Transferable Voltage Follower	Hiroki Sato, Motoki Nagata, Akira Hyogo, and Keitaro Sekine (Tokyo University of Science)

Session Chairman	Day	Time	Title	Author
Poster Session Chair: Shigetaka Takagi	14	10:40	1-V Square-Root Domain Filters Design Based on Modified Electronically Simulated Translinear Loop and State-Space Approach	Yi-Ching Wu, Hsin-Hung Ou, Kuo-Cheng Yu, and Bin-Da Liu (National Cheng Kung University)
			Op-Amp-Based Filter vs CCII-Based Filter	Boonruk Chipipop, Booncharcon Sirinaovakul, Satomi Ogawa, and Kenzo Watanabe (King Mongkut's University of Technology Thonoburi)
			MOS Temperature Compensated Crystal Oscillator	Takehiko Adachi, and Shoji Izumiya (Yokohama National University)
			Frequency Detector Analysis for a Wireless LAN Frequency Synthesizer	Steffen Albrecht, Adam Strak, Yasuaki Sumi, and Mohammed Ismail (Royal Institute of Technology (KTH))
			Common-Mode and/or Differential-Mode Selecting Noise Suppression Circuits using a Three-Input Operational Amplifier	Toshiro Tsukada (Semiconductor Technology Academic Research Center)
			Design of Robust Continuous-Time Sigma-Delta Modulator with High Output Swing OTA	Junhua Shen, Kongpang Pun, Chiusing Choy, and Cheongfat Chan (The Chinese University of Hong Kong)
			Inhibitory Cell Circuit of the Neocognitron-type Artificial Neural Network	Ken Saito, and Yoshifumi Sekine (Nihon University)
			Mixed-Signal-Implementation of a Path Searcher for UMTS Mobile Radio	S. Linzmajer, A. Graupner, and R. Schuffny (Dresden University of Technology)
			A new Approach to Identification and Correction of Structural Modelling Errors in Conservative VHDL-AMS Modells	Abdulhadi Shoufan, and Sorin A. Huss (Darmstadt University of Technology)
Lunch		12:30		
Converter 1 Chair: Akira Yasuda & Seng-Pan U	14	13:30	Systematic Analysis of Unstable Reference Voltage Induced Distortion Effects in Very-High-Speed Pipelined A/D Converters	Weng-Ieng Mok, Pui-In Mak, Seng-Pan U, and R. P. Martins (University of Macau)
		13:50	An Improved Binary Algorithmic A/D-converter Architecture	Svante Signell, and Liviu Chiaburu (Royal Institute of Technology (KTH))
		14:10	Differential Pipelined Rail-to-Rail ADC consisting of Two-MOSFET's circuitry	Kawori Takakubo, Kazuo Shimizu, and Hajime Takakubo (Meiji University)
		14:30	Gain Error Correction in Pipeline ADCs with Digital Reddundancy	Antonio J. Gines, Eduardo J. Peralias, and Adoracion Rueda (Centro Nacional de Microelectronica (I.M.S.E.))
		14:50	Distortion in Pipelined Analog-to-Digital Converters	Johan Piper, and Jiren Yuan (Lund University)
		15:10	Low-Power Design of 10-bit 80-MSPS Pipeline ADCs	Tomohiko Ito, Daisuke Kurose, Takeshi Ueno, Takafumi Yamaji, and Tetsuro Itakura (Toshiba Corporation)
Coffee Break		15:30		
Converter 2 Chairs: Akira Yukawa & Pui-In Mak	14	15:50	Novel Low Jitter Multi-Phase Clock Generation Scheme for Parallel Analog-to-Digital Conversion Systems	Sai-Weng Sin, Seng-Pan U, and R. P. Martins (University of Macau)
		16:10	Influence the High Order Distortion of the Integrator in Continuous-time Band-pass ΔΣADC Output	Rintaro Fujita, Akira Hyogo, and Keitaro Sekine (Tokyo University of Science)
		16:30	A 1-V 2.56-MHz Clock-Rate CMOS Multi-bit ΔΣ Modulator with Reset-Opamp Technique and Pseudo Data-Weighted-Averaging for Portable Audio Data Acquisition System	Hon-Weng Chong, Kai-Yiu Che, Seng-Pan U, and R. P. Martins (University of Macau)
		16:50	A 1-V 5.12-MHz Sampling-Rate 13-bit CMOS ΔΣ Modulator Using Reset-Opamp Technique for Portable Audio Data Acquisition System	Kai-Yiu Che, Hon-Weng Chong, Seng-Pan U, and R. P. Martins (University of Macau)
		17:10	A Cascaded Delta-Sigma DAC using Analog FIR Filter with a New Mismatch Shaper	Akira Yasuda, Koichi Sato, Masahiro Shibata, and Soga Tsuyoshi (Hosei University)
		17:30	Low Power 12-bit Digital-to-Analog Converter Module for Bluetooth Applications	Bhanudeep S. Bindra, A. Stojcevski, and J. Singh (Victoria University)
Banquet	14	18:30		

Session Chairman	Day	Time	Title	Author
Communication and Intelligent System 1 Chair: Nobukazu Takai	15	9:00	A 20GHz Wide Locking Range Injection-Locked Divide-by-Two Circuit	Chia-Huang Fu, and Chorng-Kuang Wang (Nationl Taiwan University)
		9:20	A 1.3 Gb/s LVDS I/O Interface with On-Chip Calibrated Terminator	Bill M.P. Lam (Fujitsu Microelectronics America)
		9:40	A 125 MHz Analog Equalizer with Baseline Wander Cancellation for 1000BASE-T Receiver Front End	Fu-Chien Huang, Chih-Chien Hung, Jyh-Yih Yeh, Tai-Cheng Lee, and Chorng-Kuang Wang (National Taiwan University)
		10:00	A Multistandard Transmitter D/A Interface with Embedded Frequency Up-Conversion and Two-Step Channel Selection	Ka-Hou Ao Ieong, Chong-Yin Fok, Seng-Pan U, and R. P. Martins (University of Macau)
Coffee Break		10:20		
Communication and Intelligent System 2 Chairs: Toshiro Tsukada & Peng-Un Mak	15	10:40	A Complex Low-IF Transceiver Architecture for Relaxing Phase Noise and Settling Time of RF Frequency Synthesizer	Pui-In Mak, Ka-Hou Ao Ieong, Chong-Yin Fok, Seng-Pan U and R. P. Martins (University of Macau)
		11:00	A Smart RF ID Tag Circuit for Mouse's Heartbeat Signal Extraction	Toshitaka Yamakawa, Takahiro Inoue, Shinichirou Eto, Tomoya Takenaka, Junichi Chiyoyaga, and Akio Tsuneda (Kumamoto University)
		11:20	A Multifunctional CMOS A/D Interface for Low-IF/Zero-IF Reconfigurable Multistandard Wireless Receiver	Pui-In Mak, Seng-Pan U, and R. P. Martins (University of Macau)
		11:40	Temporal Pattern Recognition Circuit Using Hardware Ring Neural Networks	Katsutoshi Saeki, Atsufumi Takeda, and Yoshifumi Sekine (Nihon University)
		12:00	A Low Power CAM using Pass transistor Adiabatic Logic	G.Josemin Bala, and J. Raja Paul Perinbum (Anna University)
Lunch		12:20		
Amplifier Chairs: Kimiyoshi Mizoe & Sai-Weng Sin	15	13:30	A Compact Low-Voltage High-Power-Efficient CMOS Operational Amplifier with Rail-to-Rail Output Stage	Yoshimitsu Takahashi, Akira Hyogo, and Keitaro Sekine (Tokyo University of Science)
		13:50	A High Gain Bandpass Amplifier for RF Applications	Ro-Min Weng, and Pei-Shan Lin (National Dong Hwa University)
		14:10	A Simple, Low Voltage OTA Based on MOS Cascode Current Mirror	Hiroki Sato, Akira Hyogo, and Keitaro Sekine (Tokyo University of Science)
		14:30	2.5 Gb/s, 72 dBΩ Transimpedance Amplifier in 0.35 μm CMOS	Hakan Bengtson, and Christer Svensson (Linkopings Universitet)
		14:50	A Low Voltage 5.2 GHz LAN with an On-Chip Image Filter	Stephen Knox, John W. M. Rogers, and N. Garry Tarr (Carleton University)
		15:10	Analysis of Common-Mode Parasitic Oscillation in a Wideband IQ Modulator with Multi-Stage Differential Amplifiers	Kiyoyuki Ihara (Taiyo Yuden R&D Center of America)
Coffee Break		15:30		
Modeling, Design & Test Chairs: Kazuyuki Wada & Man-Chong Wong	15	15:50	An Accurate Circuit Model for a General Sample-and-hold Circuit	Gang Xu, and Jiren Yuan (Lund University)
		16:10	A CMOS Continuous-Time FPAA Analog Core Using Automatically-Tuned Linear MOS Resistors	Jun Yasunari, Takahiro Inoue, Hiroyuki Fuchigami, and Akio Tsuneda (Kumamoto University)
		16:30	AHDL Behavioral Model of Track and Hold Amplifiers For High-Speed High-Resolution ADC	Devrim Y. Aksin, and Franco Maloberti (University of Texas at Dallas)
		16:50	MEMS Design for LSI Tester Applications	Masashi Kono, Takanori Komuro, Haruo Kobayashi, Keigo Kimura, Hiroshi Sakayori, and Yuzo Yasuda (Gunma University)
		17:10	The Design and Test of A CMOS Readout IC for Microbolometer IR FPA	Yung-Chih Liang, and Meng-Lieh Sheu (National Chi-Nan University)
		17:30	Connecting Design&Test in analog/mixed-signal integrated circuits: the case of Oscillation-Based Test	G. Huertas, D. Vazquez, A. Rueda, and J.L.Huertas (Instituto de Microelectronica de Sevilla (IMSE-CNM))
		17:50	A Strategy for Testing Analogue Circuits and Systems Embedded into SoC	HJ Kadim (Liverpool JM University)
Closing	15	18:10	Closing Ceremony	